THE ASSESSMENT OF LOGMOD AS A TESTABILITY DESIGN TOOL

Prepared for:

Chairman, Joint Logistic Commanders Panel on
Automatic Testing

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Testability Subtasks

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FOREWORD

LOGMOD (Logic Model) is an engineering design and maintenance troubleshooting tool developed by Dr. Ralph De Paul, Jr. of DETEX Systems, Inc., Villa Park, California.

On 21 March 1980 the Interservice Group on the Exchange of Technical Manual Technology, chaired by W. J. Stiegmann, completed an evaluation of LOGMOD. This group found that the LOGMOD methodology offered an opportunity to perform accurate troubleshooting of complex systems with a reduction in required test time. The group also recommended that the design aspects of LOGMOD be examined by a parallel interservice group, the Joint Commanders Panel on Automatic Testing.

The JLC Panel on Automatic Testing held its annual program review on 9-13 June 1980 and at that time invited Dr. De Paul to present his approach to the Testability task group. The LOGMOD approach was determined by the task group to have merit as a design tool for improving the testability of weapon systems. In particular, the LOGMOD system was determined to have great potential for making the test generation process more effective and less costly.

The evaluation of LOGMOD as a testability tool was incorporated as a mile-stone in the RADC Testability Program (JLC Subtask 30304) scheduled for completion in September 1981. In order to provide timely information on the testability design aspects of LOGMOD, this report has been prepared to present the status of the JLC Panel assessment of LOGMOD as of 31 December 1980.

BACKGROUND

Several evaluations of the DETEX Logic Model and Maintenance Aid (interactive test set) for troubleshooting large complex systems have been conducted in the past few years. A list of completed and ongoing evaluations is given in Table 1. The application of the Maintenance Aid to several systems has shown that the Logic Model Approach can simplify the troubleshooting problem and reduce the skill levels required to perform the required maintenance testing.

Brief descriptions of the Logic Model concept and the Maintenance Aid hardware are given in enclosure (1). The completed evaluations are well documented and the results are not repeated here. It is also important to note that the previous evaluations essentially addressed the effectiveness of manual troubleshooting procedures when aided by an "automated technical manual" (the DETEX Maintenance Aid). The JLC Panel evaluation deals only with the potential of LOGMOD to provide guidance during the initial design of a weapon system in order to make the system more testable (design for testability).

The JLC Panel on Automatic Testing coordinates more than eighty major sub-tasks being performed by the Army, Navy and Air Force including ten subtasks dealing with Design for Testability. Enclosure (2) is a preprint of a paper to be given at the Annual Reliability and Maintainability Symposium which describes the JLC Program in Design for Testability. Considerable detail is devoted to the Rome Air Development Center (RADC) Testability Program under which the LOGMOD testability evaluation is being performed. It may be noted that although the JLC Panel addresses automatic testing issues, the Design for Testability subtasks also address weapon systems designs which better support manual testing methods (such as the LOGMOD approach). There is also the potential to adapt the LOGMOD approach for use in fully automated test environments.

Table1. LOGMOD Evaluations

Maintenance Aid (Test Set)

Completed and Documented Evaluations

Final Report, LOGMOD Diagnostic Test Set Demonstration, US Army Air Mobility Research and Development Laboratory, Moffett Field, June 1977.

Final Report, LOGMOD Diagnostics, Project 760701, Air Force Logistics Management Center, 15 October 1978.

LOGMOD Final Report, Interservice Group on the Exchange of Technical Manual Technology, 21 March 1980.

Ongoing Evaluations

Sperry, Great Neck NY, for Air Force Modular Automatic Test Equipment (MATE) Program.

Lockheed, Sunnyvale CA, for production line tester for Navy Trident missile components.

Naval Air Engineering Support Office, San Diego CA, for depot testing of Navy E-2C aircraft avionics.

Naval Ship R&D Center, Carderock MD, for Navy Technical Information Presentation System (NTIPS).

Design for Testability Ongoing

Evaluations

Army Advanced Technology Laboratory, Ft. Eustis, VA, for TOW missile built-in test.

Naval Air Engineering Center, Lakehurst NJ, on applicability of LOGMOD to automatic testing.

Rome Air Development Center, Rome NY, on use of LOGMOD as a testability tool (JLC Subtask 30304).

PERSPECTIVE ON MAINTENANCE AID EVALUATIONS

The DETEX Maintenance Aid, based upon the Logic Model concept, has had good success when compared against traditional testing methods. This is perhaps an indication of the expected superiority of a standardized, methodical, automated approach over an ad hoc, manual approach. As an example, LOGMOD has uncovered cases in existing test sequences where "terminal events" (out-put pins) are not inspected for correctness. This is an obvious and serious deficiency: yet in the midst of manually generating tests for a complex board, someone neglected to do the obvious. The analysis of test completeness is a natural application of an automated tool such as LOGMOD. In addition to identifying incomplete test sequences, LOGMOD has also uncovered deficient designs (sneak paths) and deficient built-in test implementations.

The utility of LOGMOD is most apparent when troubleshooting permits testing for static conditions at the test nodes. For example, in a certain equipment and under certain circumstances, the voltage at a particular node should be +28 volts ±10 percent. If the measured voltage is not within tolerance, the LOGMOD Dependency charts provide an excellent basis for directing the technician to look at other nodes in the equipment to effect fault isolation and component repair. The components here are typically switches and relays. However, in dealing with components which have complex transfer functions (such as servomechanisms and many digital circuits) static testing is only a small part of the functional testing; LOGMOD does not give any assistance in defining what the test stimulus must be (voltages, frequencies, phases, waveforms) nor what the acceptable test response should be (including tolerances). Hence, when a statement is made that LOGMOD can provide a "test strategy", it must be understood that what is provided is a test sequence ordering and that the test engineer must, as always, develop the required stimulus/response data.

LOGMOD AS A TESTABILITY TOOL

LOGMOD is a method of uniquely defining the interrelationships between the elements of a system (electronic, mechanical, hydraulic, etc.). These interrelationships are depicted on a unique logic chart. Once a Logic Model of a system has been formulated, there are several operations that can be performed on the Logic Model to address critical design issues. Fundamental questions such as the number of test points required in a system, the time to fault isolate, the cost of using alternate strategies, and the order of inspection at the test points can be addressed. The answers to these types of questions are often difficult to generate and often remain unknown or guesses at best. The Logic Model provides a "thumbprint" of the system design that serves as the basis for allowing quick, accurate, and inexpensive engineering analysis to be performed.

The effect of maintenance strategies or policies on the system can be addressed by a designer. The Logic Model provides a tool for finding out how many measurement steps are required to effect a diagnosis if a certain item should fail. The number of steps may then be compared for different design options. If automatic test equipment is required for the system, then the Logic Model can be used to determine which tests should be made automatically and which tests should be made manually or in a semiautomatic mode. Since the same structured logic is used in the design analysis as in the development of the maintenance support equipment, it is possible to have the troubleshooting approach and maintenance procedures completed by the time the first system is operational. This can eliminate the lag that always seems to exist between the completion of system design and the completion of support equipment design. Some of the issues which may be analyzed through LOGMOD include:

a. The design allowables (what events can be tested).

b. The economic analysis of the test alternatives.

c. The maintenance philosophy (what to repair, what to throwaway).

d. The level or hierarchy of diagnosis.

e. The use of automatic vs. manual test.

f. Making the best use of the human operator in effecting a diagnosis.

PRELIMINARY EVALUATION OF LOGMOD AS A TESTABILITY TOOL

One of the most important aspects of the LOGMOD system is it is always results in the most optimum method of both fault detection and fault isolation. It has been mathematically shown that the partial order set theory used in the Logic Model concept constitutes the basis for creating trouble-shooting procedures which are extremely efficient. No other test procedure presently known has been found to date that can find a malfunction in a more efficient manner. The technique can also be used as a design tool to ensure that a system under design will, when committed to hardware, be both testable as well as operable. The technique is not a panacea; it cannot do things people cannot do. As an example: if a feedback loop is found (the system will find such loops), then the loop must be broken if the internal functions are to be tested.

In the process of automating LOGMOD, the actual computer program is also unique in that it is a heuristic rather than deterministic program. A heuristic program will always be more efficient than an equivalent deterministic program. However, in practice it is much more difficult to generate a heuristic program and as a result they are seldom used. Using the LOGMOD logic chart, heuristic programming becomes as easy as the usual deterministic techniques.

LOGMOD and the Maintenance Aid work only as well as the weapon system design permits. LOGMOD and any other troubleshooting approach will always provide good diagnostic resolution when an unlimited number of test points are available for probing. Conversely, neither LOGMOD nor any other troubleshooting approach can hope to provide good fault diagnosis if critical test points are not available to either (1) an automatic tester through edge connectors or (2) manual probing because of conformal coating or poor accessibility. The number of input and output pins on an edge connector which are specifically dedicated to testing is usually greatly restricted, especially in airborne systems. LOGMOD, as a testability tool, can assist in the optimum allocation of these scarce resources during the design phase. It can identify those internal circuit nodes which absolutely must be brought out to the connector pins in order to allow a minimum level of fault diagnosis. Similarly, it can identify those internal circuit nodes which are redundant to other nodes in a diagnostic sense and should not be brought out to connector pins. Finally, LOGMOD can provide quantitative data on the benefits to be derived from adding test points. These data may be used to convince engineering management to add pins for test purposes.

Using LOGMOD during the design phase imposes a desirable discipline upon the design process which demands that maintenance data, test data and reliability data be integrated with the usual performance data. The very act of methodically going through a complex circuit, assigning functional partitions and identifying dependencies is a useful exercise for providing design insight. This is true independent of whether the resulting analysis of data is automated or not.

The bringing together of performance data and test data is presently accomplished much later in the design phase at the point in time when a Test Requirements Document (TRD) is prepared. In reality, the data integration for a TRD is after the fact: the equipment is built and there is little or no opportunity for test requirements to influence equipment design. The TRD (covered by MIL-STD-1519 and MIL-STD-1345) requires data in initialization requirements, test dependencies, failure modes, and critical parameters as well as information on test equipment and test fixture requirements.

As desirable as it is to standardize on the documentation of test requirements, the existing military standards do not address requirements for test quality nor a procedure for verifying test quality. Here, a time-phased utilization of LOGMOD data and TRD data as part of the overall test requirements analysis could result in high-quality test and diagnostic procedures, whether manual or automated. LOGMOD analysis and TRD generation require essentially the same design data on the Unit Under Test (UUT). The data used by LOGMOD would necessarily be preliminary in nature and subject to update and repeated analysis. Using this UUT engineering data, LOGMOD can identify design deficiencies with respect to testing which can be rectified prior to the

design being "frozen". It can guide the test designer toward a test strategy that is both complete and contains an optimum number of test steps, subject to design and testing constraints.

The actual test stimulus and response data (corresponding to LOGMOD "messages") would be generated by the best means available and not limited to manual means as is now done for the LOGMOD Maintenance Aid. Use may eventually be made of Analog Automatic Test Program Generation (AATPG) software presently under development by the Naval Air Engineering Center (NAEC, Lakehurst) and the Air Force Aeronautical Systems Division (ASD, Wright-Patterson) under JLC Subtask 30201.

The LOGMOD approach to modeling circuitry as functional blocks is very appropriate for the early design phase when functional data may be the only information available. However, when generating stimulus/response data, the actual circuit structure (implementation of the function) must be taken into account in order to detect and isolate implementation-dependent failures. Thus the UUT data base for an ATPG system would necessarily be different from the data base for LOGMOD analysis. In addition, it is difficult to relate test quality specifications (e.g., percent faults detected, percent faults correctly isolated to failed component) to the LOGMOD analysis which uses functional models and functional failures. This problem is a general one and is not restricted to the LOGMOD approach.

Being a functional approach, LOGMOD is not limited to the analysis of only electronic circuits. LOGMOD appears to be equally applicable to electrical, mechanical, hydraulic and other systems. However, for electronic circuits, LOGMOD seems to deal much more adequately with single-function circuitry typical of analog systems than with multi-function circuitry typical of digital systems. As an example, it is difficult to enumerate the many dependencies between each output data line of a digital line of a digital ROM (Read-Only Memory) and each input address line.

Although the developers of LOGMOD claim that their approach is applicable to digital circuits and at least one ongoing evaluation (Navy NESO) investigates digital circuits, there are at least two circumstances which make LOGMOD/Maintenance Aid approach less valuable for digital analysis than for analog analysis.

1) In many digital ATE environments, the Maintenance Aid would be a redundant piece of equipment. Many automatic test equipments feature a guided probe capability in which the ATE software determines the next placement of the probe (same as Maintenance Aid (MA) message), automatically provides the test stimulus (a manual operation for MA), and determines if a PASS of FAIL condition exists (a manual operation for MA). Here, the only justification for including the Maintenance Aid in the field or at the depot would be as a backup for the ATE in case of an ATE malfunction.

2) In the area of testability design analysis, there are at least three digital testability analysis tools reported in the open literature: Bell Telephone Laboratory's TEAMS program, Sandia Laboratory's SCOAP program and Sperry Univac's TESTSCREEN program. Similar programs at several private companies have been developed under in-house Independent Research and Development (IR&D) funding. Most of these programs are specifically tailored to work with the data base peculiar to each company's Computer Aided Design system, including automatic test generation tools. All of these programs do a good job of analyzing the structure of the digital system to provide guidance on test point placement, partitioning, initialization techniques, etc.

In summary, depicting a digital system in terms of functional dependency chains does not offer any real insight into testing and may, in fact, be counterproductive when considering today's tools (hardware and software) for digital testing and testability analysis.

TESTABILITY STANDARDIZATION

The Services are aware that if a weapon system is to be confidently tested at low cost then attention to Design for Testability principals must be given by DoD and contractors during the early design stages of the weapon system. As a result, a new draft military standard on testability requirements proposes that contractors show, prior to hardware construction, that the design will support high-quality, low-cost testing. A summary of this standardization effort is given in enclosure (3).

The LOGMOD approach offers one way to get an early, accurate indication of any testing restrictions or difficulties associated with a design prior to prototype construction. Actually, LOGMOD offers one of the few quantitative approaches available for evaluating the potential testability of analog circuits.* As such, LOGMOD could fill a position in a matrix of tools required to evaluate testability for different design phases, for different technologies and for different levels of maintenance. In late 1980, an eleventh testability subtask was added to the JLC Automatic Test Program which attempts to identify the various computer aided design (CAD) and computer aided test (CAT) tools available in government and industry for each position in the above matrix. Pending favorable results of the RADC LOGMOD evaluation, LOGMOD will be integrated into a network of available tools under this sub-task (JLC subtask 30306).

* Another promising approach is a software system for quantitatively assigning a testability figure of merit to hybrid (analog/digital) designs which was developed by Western Electric and reported at the 1979 Cherry Hill Test Conference.

REQUIRED FUTURE EFFORT

Several modifications need to be made to the existing LOGMOD system in order to have a useful testability design and analysis tool. A partial list of required features is as follows:

1. Identification of test point locations.
    a. Specified test points which are redundant or marginal.
    b. Critical test points for GO/NO GO tests which should be made accessible to automatic test connectors or built-in test.
    c. Test points for fault isolation.
        (1) Priority list based upon test information gained.
        (2) Optimum list, given connector constraints.
        (3) Priority list of probe points.
        (4) Lists based upon failure rate data.
2. Identification of circuit components in feedback loops.
    a. Calculation of unavoidable diagnostic ambiguity resulting from loops.
    b. Identification of candidate nodes at which loops may be broken in test mode.
    c. Calculation of new diagnostic ambiguities resulting from each candidate break point.
3. Implementation of new data structure which supports the identification of multiple levels of physical design (board, equipment, system) and multiple levels of testing.

The Naval Surface Weapons Center (NSWC) is contracting DETEX Systems, Inc. to determine what effort is involved in upgrading the existing LOGMOD system to include the above testability analysis features and any other useful testability features. This initial effort will develop a software specification for a testability analysis tool, based upon LOGMOD, which will provide the basis for a follow-on implementation phase if the new program is judged to be beneficial to the Services. The decision to proceed will be a joint Navy and Air Force decision coordinated through the JLC Panel.

A second consideration which is as important as technical feasibility is the ability to place the new testability tool in the hands of those who need to use it: system prime contractors, equipment subcontractors and vendors, and government technical representatives. DETEX is also preparing some options which will make the tool available and at the same time protect its sizable investment. Availability is especially critical if this tool is to be cited by the new military standard as an acceptable testability analysis approach.

TESTABILITY STANDARDIZATION

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ABSTRACT

Most project managers, in government and industry, are aware that testing costs may be significantly reduced by the early consideration of testability in prime equipment design. In addition, techniques for testable design are generally well understood by industry and have been successfully incorporated into several products. The item that is missing in acquiring testable systems and equipments for DOD is a general framework for determining requirements, trading off alternatives, measuring progress and demonstrating compliance. An effort is underway within the Navy to promote a unified approach to dealing with testability during the conceptual, validation, and full scale development phases of equipment development, including the use of specifications and design reviews for testability parameters.

FLEET TESTING PROBLEMS

Even with the introduction of new, improved ATE, the Navy has experienced problems in having testing technology keep pace with prime equipment technology. Built-in test is often not as comprehensive as required and/or causes excessive false alarms. Testing, at all levels of maintenance, often results in high ambiguity levels for fault isolation and in long test times. As a result, operational readiness suffers and high costs are incurred for the development and support of ATE, test programs, and interface devices.

As prime equipment electronics become even more complex and more critical to Fleet operation, there is an acknowledgement that these new designs must be somehow constrained to be more easily tested or they may become completely unsupportable. Thus, Design for Testability (DFT) has become an important consideration by the Navy.

ROLE OF TESTABILITY

The subject of testability has been a popular, if sometimes nebulous, topic of discussion at several test conferences. It has been promoted as a panacea for all test problems and has been viewed as an impractical, unattainable idealism. The Industry/Joint Services Automatic Test Project (I/JSATP) in 1977-1979 perhaps made the most progress toward defining the role of testability. The I/JSATP Testability Task Group recognized that many problems in achieving testability are managerial in nature and concluded that DOD and the Services must impose verifiable testability requirements during the design process and enforce compliance if testability is to become a reality. The 1979 Joint Logistic Commanders (JLC) Automatic Test Plan reflects the considerable influence of the industry project and addresses the development of policies and procedures for managing testability, the development of testability design guides, and the development of testability military standards and specifications. It was within this overall framework that the testability standardization task was conducted.

EXISTING STANDARDS

A natural first step in considering testability standardization is to take a look at existing standards to see if "small" modifications might be all that is needed. At least six such surveys have been conducted and all are in general agreement that major modifications or complete rewrites are necessary to fill the testability gaps. The subjects of ATE compatibility and maintainability are generally well covered by existing standards but there is much that is important to testability specification, measurement, and verification that is not addressed at all.

PROPOSED STANDARD

The proposed standard, "Testability Requirements for Electronic Components, Equipments, and Systems", is extracted from a study performed by the Naval Surface Weapons Center and the Naval Ocean Systems Center for the Naval Electronic Systems Command in Washington, D. C. The standard is presently undergoing internal Navy review and initial industry review.

Some additional work on the definition of uniform testability figures of merit (TFOMs) is to be completed this year. Algorithms and procedures for determining quantitative TFOMs will be incorporated as appendices to the testability military standard as they become available.

TESTABILITY PROGRAM

The proposed standard requires that testability be considered early in the design process and strives for a "balanced" design based upon performance, cost, and supportability. If applicable to a prime system development, the standard requires that the contractor incorporate a Testability Program as an integral part of the systems engineering and design engineering efforts. Testability considerations such as ATE compatibility, observability/controllability, and partitioning are factored into the design. Built-in test features such as self-checking hardware, diagnostic software, and performance monitoring circuits are incorporated and their effectiveness evaluated.

The size and degree of formality of a contractor's Testability Program can, and should, differ from project to project. For example, if the contractor is required only to establish firm policy for his design engineers on the inclusion of reasonable testability features (using this standard as a guide-line), and the procuring agency is supportive of reasonable costs incurred as a result, then the product will most likely be testable, if not measurably so. Alternatively, requirements in this standard may be selectively applied to achieve any desired degree of demonstratable testability.

TESTABILITY REQUIREMENTS

The proposed standard imposes several testability requirements on the prime equipment design process. Two of these requirements, parts selection and functional partitioning, are discussed below to give examples of testability requirements found in the standard.

PARTS SELECTION

The testability achievable by a system or equipment is usually limited by the testability of the lowest piece parts, such as integrated circuits. This is especially true of many LSI circuits where performance and cost are emphasized and testability is not a consideration. Some industry leaders predict that this imbalance will change in the next few years. The proposed standard requires that, given comparable performance and cost characteristics, preference shall be given in the selection of integrated circuit components and assembled modules to those components and modules which have demonstrated satisfactory testability characteristics. Thus, preference will be given to those components for which sufficient disclosure of internal IC structure and failure modes have been provided for use as a basis for effective, economical testing.

FUNCTIONAL PARTITIONING

If testable design techniques could be summarized in a single phrase, that phrase might be "divide and conquer". By providing sufficient controllability and observability in a design (at least in test mode), the test generation process and the testing process for a piece of hardware can become manageable at a reasonable cost. Thus, the proposed standard requires that the prime equipment be designed such that relatively small, independent, and manageable blocks of circuitry may be defined as the basis of test derivation, test documentation, and test evaluation. The standard requires appropriate trade-offs be conducted between the benefits of testability features and increased weight, power, and unreliability due to these features. It may be noted that the trend of digital electronics toward LSI and VLSI and the potential for on-chip testability and self-test make the above negative factors less severe.

TESTABILITY ANALYSIS

The standard requires that the contractor develop models for each prime item which are to be used as the basis for testability design, analysis, and evaluation. During preliminary design, the models address the hardware structure of equipments and their modules, stressing test control and test access for internal components. During detail design, the models are refined to provide design feedback to hardware designers and test designers. Testability techniques, models, analysis methods and qualitative and quantitative effectiveness data are presented at normally scheduled design reviews.

DATA

The proposed standard calls for a new data item, the Testability Analysis Report. The report is to be submitted twice, once at the Preliminary Design Review and once at the Critical Design Review, for government review and approval. It is anticipated, however, that the report's greatest usefulness will be realized within the contractor's own facility as the interfacing document between design engineers, test engineers, software personnel, and sub-contractor personnel.

During preliminary design, the Testability Analysis Report documents testability requirements, design trade-offs, test strategies, and a functional description of built-in test features (hardware and software) and testability features for each item. It also identifies the failure modes to be addressed by the test process and proposed methods for evaluating test effectiveness.

During detail design, the Testability Analysis Report is more quantitative in nature. It addresses the testing of the prime item as UUTs on an ATE and also addresses the built-in testing of the prime item. In the former case the data supports the Test Requirements Analysis for each UUT and in the latter case the data supports the development of diagnostic self-test software. The report includes the quantitative analysis of the failure detection and failure isolation predicted for external test and BIT.

TESTABILITY DEMONSTRATION

The standard requires that the contractor conduct a testability demonstration as a part of the overall qualification testing for the prime system and for each equipment. The demonstration samples and measures the effectiveness of built-in test hardware, diagnostic software, and testability features. The demonstration is also used to validate the models used in the more comprehensive testability analysis. The validation is achieved by the insertion of faults into hardware and the application of the test stimulus using built-in test and off-line testers. The results of the demonstration are documented in the Testability Analysis Report. Any serious deficiencies identified may result in a redesign of the prime system, the test system, or both.

CONCLUSION

In today's environment of increasing prime equipment complexity, it is no longer enough to consider testability as simply a desirable characteristic or as a design goal. Testability must take its place as an absolute condition of prime equipment acceptance with quantifiable requirements and evaluation criteria. It is believed that the testability standardization study and the resulting proposed standard have contributed toward making this a possibility.